

APPLICANT(S): DIECKROGER, Jens et al.  
SERIAL NO.: 10/075,536  
FILED: February 14, 2002  
Page 5

### **REMARKS**

The present Amendment is intended to be fully responsive to all points of objection and/or rejection raised by the Examiner and is believed to place the application in condition for allowance. Applicants assert that the present invention is new, non-obvious and useful. Prompt consideration and allowance of the claims are respectfully requested.

### **Status of Claims**

Claims 1-2 and 4-20 are pending in the application.

Claims 14-16 have been allowed.

Claims 1, 2, 4-13, 17-20 have been rejected.

Claims 1, 14 and 17 have been amended herein. Such amendments are variously intended to more clearly define what Applicants regard to be the invention, clarify the scope of the claims or correct typographical errors. It is respectfully submitted that no new matter is added.

### **Allowable Subject Matter**

Applicants are grateful to the Examiner for indicating the allowability of claims 14-16.

### **CLAIM REJECTIONS**

#### **35 U.S.C. § 102 Rejections**

The Examiner rejected claims 1-3 under 35 U.S.C. § 102(b), as being anticipated by Hirataka et al. (EP0723171). The Examiner contended that Hirataka discloses an optical module having an optical channel, a trench in the circuit for interrupting the optical channel, and a detection unit disposed in the trench for detecting optical signals in the channel. The

APPLICANT(S): DIECKROGER, Jens et al.  
SERIAL NO.: 10/075,536  
FILED: February 14, 2002  
Page 6

Office Action further states that the detection unit includes a support submount including metal electrodes and solder bumps. Applicants respectfully traverse these rejections in view of the remarks that follow.

It is well-established that a rejection under 35 U.S.C. § 102 is only properly made if the reference discloses each and every element of a claim. Applicants respectfully submits that Hirataka does not disclose each and every element of amended independent claim 1. Specifically, Hirataka does not disclose, at least, “a support submount attached to said planar light circuit”, or any structure that can be reasonably be construed to anticipate such element of amended claim 1. The Examiner has argued in the Office action that “support submount could be any elements of elements 6, 7 and/or 8[.]” Applicants continue to argue that Hirataka does not disclose the configuration of claim 1. Rather, Hirataka describes a photodiode and a planar light circuit; and there is no teaching of Hirataka of a support submount or similar element attached to the planar light circuit.

In any event, even if the solder bumps of Hirataka may be considered to be a support submount – which they cannot be – then there is certainly no teaching in Hirataka of a “support submount attached to said planar light circuit outside said trench” as recited in amended claim 1. Rather, Hirataka shows the photodiode being attached directly to the planar light circuit inside the trench. Accordingly claim 1 as amended is not anticipated.

In view of the above, it is respectfully submitted that amended claim 1 is not anticipated by Hirataka. Furthermore, it is respectfully submitted that amended independent claim 1 is patentable over Hirataka, alone or in combination with any other prior art reference. The Hirataka reference and other prior art cited by the Examiner teach attaching the detection unit directly to the planar light circuit, thereby teaching away from including a support submount and attaching the detection unit to said submount.

The Examiner further rejected claims 1-8, 10, 11, 17 and 18 under 35 U.S.C. § 102(b), as being anticipated by Yamamoto et al. (EP0807981). The Examiner has contended that the Yamamoto reference discloses an optical module comprising a planar light circuit having optical channels, a trench formed in the planar light circuit for interrupting the optical channels and a detection unit with photodiodes disposed in the trench for detecting optical

APPLICANT(S): DIECKROGER, Jens et al.  
SERIAL NO.: 10/075,536  
FILED: February 14, 2002  
Page 7

signals in the channels. The Office Action further states that the detection unit is mounted on a support transparent substrate by solder bumps and electrodes including a common electrode. Applicants respectfully traverse these rejections in view of the remarks that follow.

It is well-established that a rejection under 35 U.S.C. § 102 is only properly made if the reference discloses each and every element of a claim. Applicants respectfully submits that Yamamoto does not disclose each and every element of amended independent claim 1. Specifically, as discussed with respect to Hirataka, above, Yamamoto does not disclose, at least, “a support submount attached to said planar light circuit”, or any structure that can be reasonably be construed to anticipate such element of amended claim 1. Rather, Yamamoto states that “the optical module 301 includes the optical waveguide 13 on the support substrate 1 and further a photoreception device 401 is mounted directly on the support substrate.” (col. 18 lines 7-11) (emphasis added); see also, e.g., Fig. 4A, showing photoreception device attached directly to planar light circuit.

In any event, even if the solder bumps of Yamamoto may be considered to be a support submount – which they cannot be – then there is certainly no teaching in Yamamoto of a “support submount attached to said planar light circuit outside said trench” as recited in amended claim 1. Rather, Yamamoto shows the photodiode being attached directly to the planar light circuit inside the trench. Accordingly claim 1 as amended is not anticipated.

In view of the above, it is respectfully submitted that amended claim 1 is not anticipated by Yamamoto. Furthermore, it is respectfully submitted that amended independent claim 1 is patentable over Yamamoto, alone or in combination with any other prior art reference. The Yamamoto reference and other prior art cited by the Examiner teach attaching the detection unit directly to the planar light circuit, thereby teaching away from including a support submount and attaching the detection unit to said submount.

Likewise, with respect to independent method claim 17, Applicants respectfully traverse the rejection. As discussed above, Yamamoto does not teach or disclose a support submount for a detection unit. Specifically, Yamamoto does not disclose at least the method elements of “providing a support submount,” “mounting a detection unit on the support

APPLICANT(S): DIECKROGER, Jens et al.  
SERIAL NO.: 10/075,536  
FILED: February 14, 2002  
Page 8

submount,” or “placing the support submount on the planar light circuit outside said trench using flip-chip mounting.” Accordingly, Yamamoto does not perform, either expressly or inherently, all elements of claim 17. Therefore, claim 17 and its dependent claim 18, are patentable over Yamamoto.

Finally, Applicants call the Examiner’s attention in particular to claims 19 and 20, which were not specifically referred to the Office action. It is respectfully asserted that the prior art of record does not teach the configuration “wherein said support submount is attached to said planar light circuit by flip-chip mounting” as recited in claim 19. Nor does the prior art of record teach the configuration “wherein said detection unit is not directly attached to said planar light circuit” as recited in claim 20.

Accordingly, based at least on the above, Applicants respectfully assert that independent claims 1 and 17 are allowable. Moreover, claims 2, 4-8, 10, 11, 17-20, which depend directly or indirectly therefrom, are likewise allowable. Accordingly, Applicants respectfully request that the Examiner withdraw the rejections to the pending claims.

### **35 U.S.C. § 103 Rejections**

In the Office Action, the Examiner rejected claims 9, 12 and 13 under 35 U.S.C. § 103(a), as being unpatentable over Yamamoto (EP0706981). Applicants respectfully traverse the rejection because a prima facie case of obviousness has not been established vis-à-vis amended claim 1. A prima facie case obviousness rejection must at least show the express or inherent presence of each and every element of a claim in the prior art. Without conceding to the propriety of the Examiner’s argument for obviousness, which failed to refer to a specific reference from the art, by which the Examiner modified the teachings of the Yamamoto reference, or the lack of motivation to do so, Applicants respectfully assert that the cited prior art does not contain each and every element of claim 1.

In view of the foregoing remarks and arguments, it is respectfully asserted that the cited prior art fails to teach or otherwise render obvious all elements of independent claim 1, and specifically “a support submount attached to said planar light circuit”, or “a detection unit disposed on said support submount to detect optical signals in said optical channel.”

APPLICANT(S): DIECKROGER, Jens et al.  
SERIAL NO.: 10/075,536  
FILED: February 14, 2002  
Page 9

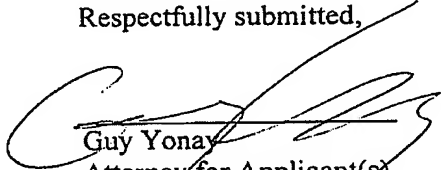
In view of the non-obviousness of independent claim 1, dependent claims 9, 12, and 13, which depend directly or indirectly therefrom, should likewise be allowed.

In view of the foregoing amendments and remarks, the pending claims are deemed to be allowable. Their favorable reconsideration and allowance is respectfully requested.

Should the Examiner have any question or comment as to the form, content or entry of this Amendment, the Examiner is requested to contact the undersigned at the telephone number below. Similarly, if there are any further issues yet to be resolved to advance the prosecution of this application to issue, the Examiner is requested to telephone the undersigned counsel.

Please charge any fees associated with this paper to deposit account No. 05-0649.

Respectfully submitted,



Guy Yonay  
Attorney for Applicant(s)  
Registration No. 52,388

Dated: August 11, 2004

**Eitan, Pearl, Latzer & Cohen Zedek, LLP.**  
10 Rockefeller Plaza, Suite 1001  
New York, New York 10020  
Tel: (212) 632-3480  
Fax: (212) 632-3489